CLAIMS

What we claim is:

1. A method comprising:

determining at least one characteristic of a first input/output (I/O) device that is coupled to a memory device interface, the memory device interface being configured to enable data transfers between the I/O device and a memory device; and

buffering data corresponding to the first I/O device in a first portion of a buffer of the memory device interface, a size of the first portion being responsive to the at least one characteristic of the first I/O device.

2. The method of claim 1, further comprising:

determining at least one characteristic of a second I/O device that is coupled to the memory device interface; and

buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at least one characteristic of the second I/O device.

3. The method of claim 2, further comprising:

receiving data from the first I/O device via a first data transfer link; and

receiving data from the second I/O device via a second data transfer link.

4. The method of claim 2, further comprising:

receiving a first data unit from the first I/O device;

buffering the first data unit in the first portion of the buffer; and

transferring the first data unit to the memory device;

receiving a second data unit from the second I/O device;

buffering the second data unit in the second portion of the buffer; and

transferring the second data unit to the memory device.

5. The method of claim 1, wherein the at least one characteristic comprises at least one of:

a rate at which the I/O device is able to read data from the memory device;

a rate at which the I/O device is able to write data to the memory device;

a bandwidth of a link coupled between the I/O device and the memory device interface;

a size of a data unit that the I/O device reads from the memory device per read request;

a size of a data unit that the I/O device writes to the memory device per write request;

a tolerance that the I/O device has for a delay by the memory device interface in fulfilling a write request; or

a tolerance that the I/O device has for a delay by the memory device interface in fulfilling a read request.

6. A method for allocating buffer capacity in a memory device interface that is configured to transfer data between an input/output (I/O) device and a memory device, the method comprising:

buffering data received via a first data transfer link in a first portion of a buffer of the memory device interface;

buffering data received via a second data transfer link in a second portion of the buffer, a buffering capacity of the first portion being different than a buffering capacity of the second portion.

7. The method of claim 6, wherein the buffering capacity of the first portion is responsive to at least one characteristic of a first I/O device that provides data to the memory device interface via the first data transfer link, and the buffering capacity of the second portion is responsive to at least one characteristic of a second I/O device that provides data to the memory device interface via the second data transfer link.

8. The method of claim 7, further comprising:

receiving a first data unit from the first I/O device via the first data transfer link;

buffering the first data unit in the first portion of the buffer;

transferring the first data unit to the memory device;

receiving a second data unit from the second I/O device via the second data transfer link;

buffering the second data unit in the second portion of the buffer; and

transferring the second data unit to the memory device.

9. The method of claim 7, further comprising:

receiving a first data unit from the memory device;

buffering the first data unit in the first portion of the buffer;

transferring the first data unit to the first I/O device;

receiving a second data unit from the memory device;

buffering the second data unit in the second portion of the buffer; and

transferring the second data unit to the second I/O device.

10. A memory device interface that is configured to enable data transfers between an input/output (I/O) device, the memory device interface comprising:

a buffer;

a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data corresponding to a first I/O device; and

a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data corresponding to a second I/O device, a size of the first portion of the buffer being different than a size of the second portion of the buffer.

11. The memory device interface of claim 10, wherein the buffer comprises random access memory (RAM).

12. The memory device interface of claim 10, wherein the first plurality of registers comprises:

a first buffer allocation counter that specifies a buffer allocation value that is configured to enable data received from the first I/O device to be buffered in the first portion of the buffer; and

a second buffer allocation counter that specifies a buffer allocation value that is configured to enable data received from the second I/O device to be buffered in the second portion of the buffer.

13. The memory device interface of claim 12, wherein the value of the first buffer allocation counter is decremented responsive to a buffer allocation value being sent to the first I/O device.

14. The memory device interface of claim 13, wherein the value of the first buffer allocation counter is incremented responsive to data being read from the first portion of the buffer.

15. A memory device interface comprising:

a buffer;

a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data received via a first data transfer link; and

a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data received via a second data transfer link, a size of the first portion of the buffer being different than a size of the second portion of the buffer.

16. The memory device interface of claim 15, wherein the buffer comprises random access memory (RAM).

17. The memory device interface of claim 15, wherein the first data transfer link is coupled to a first input/output (I/O) device, and the second data transfer link is coupled to a second I/O device.

18. The memory device interface of claim 15, wherein the first plurality of registers comprises:

a first buffer allocation counter that is configured to enable data received via the first data transfer link to be buffered in the first portion of the buffer; and

a second buffer allocation counter that is configured to enable data received via the second data transfer link to be buffered in the second portion of the buffer.

19. A system comprising:

means for determining at least one characteristic of a first input/output (I/O) device that is coupled to a memory device interface, the memory device interface being configured to enable data transfers between the I/O device and a memory device; and

means for buffering data corresponding to the first I/O device in a first portion of a buffer of the memory device interface, a size of the first portion being responsive to the at least one characteristic of the first I/O device.

20. The system of claim 19, further comprising:

means for determining at least one characteristic of a second I/O device that is coupled to the memory device interface; and

means for buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at least one characteristic of the second I/O device.